AN1233
Application note

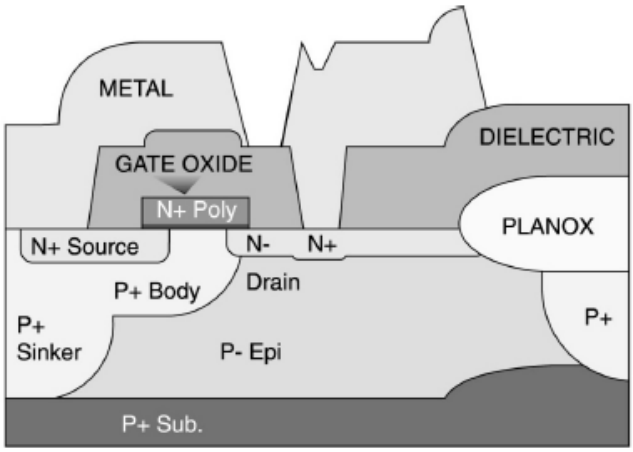
LDMOS packages

Introduction

LDMOS technology recently implemented at ST is an important step forward, combining technological and environmental progress. In the basic LDMOS structure (*Figure 1*), a p-epitaxial layer is grown on an p-type substrate to form a larger drain region. An important consequence of this structure is that both the n+ source and the drain region are on the die surface, with the laterally diffused low resistance p+ sinker connecting the source region to the p+ substrate and source terminal. Wire-bonded connections which normally connect the source and the external circuitry (DMOS configuration) are no longer required, thus greatly reducing negative feedback due to the self-capacitance and inductance of the wires. This leads to higher gain at high frequencies. A further advantage of this structure is that an electrical insulator required to isolate the drain with DMOS transistors is no longer needed. Not only are electrical and thermal performances of the package improved, but beryllium oxide, a toxic compound, is also eliminated from the package. LDMOS package development offers higher dissipated power, cost reduction, and lower environmental impact.

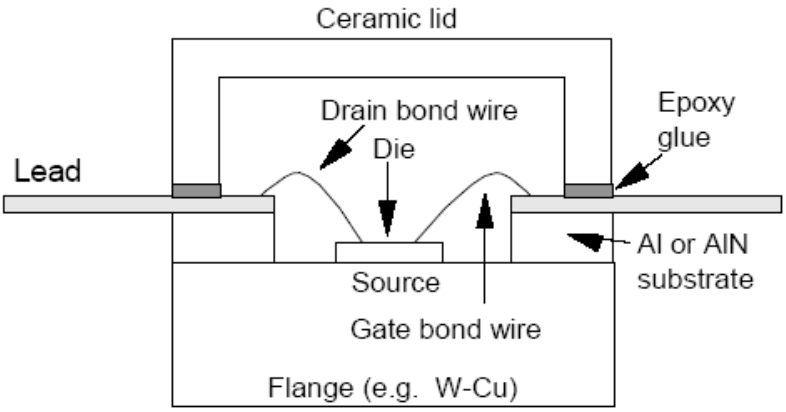
1 LDMOS package structure

Figure 1. LDMOS cross section



In such a structure there is no need to electrically isolate the die from the flange as for bipolar die, by using a Beryllium Oxide (BeO) interface (*Figure 1* and *Figure 2*). LDMOS package development eliminates any substances which could affect and/or deteriorate the environment. Because BeO is toxic, it is no longer used. The LDMOS die is soldered directly to the flange (for example, the tungsten-copper alloy flange) which results in better electrical and thermal performances.

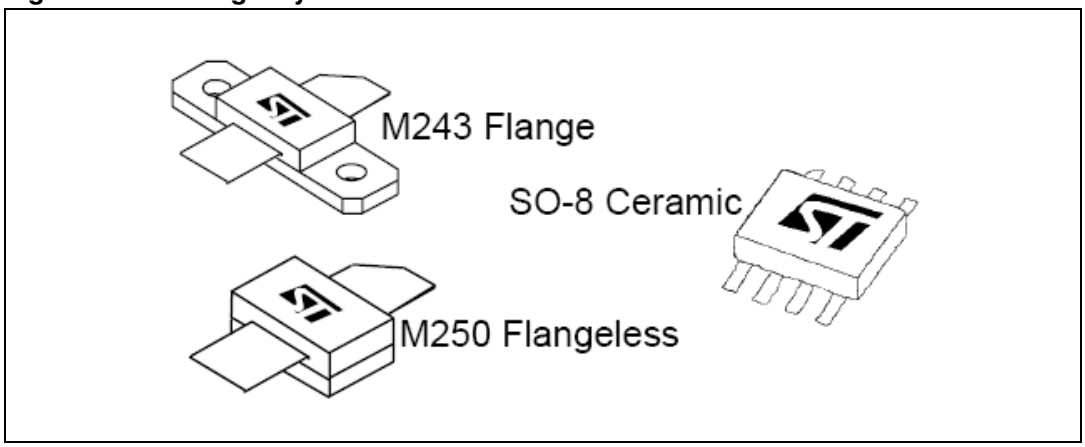
Figure 2. LDMOS package structure



2 Mounting techniques and characteristics

Surface mount packages were developed to reduce assembly cost and space allocation on printed circuit board (PCB). Today, ST microelectronics offers three types of packages for its L-DMOS product: Flange, Flangeless and SMD (*Figure 3*). All three package types have their own mounting techniques and characteristics.

Figure 3. Package styles

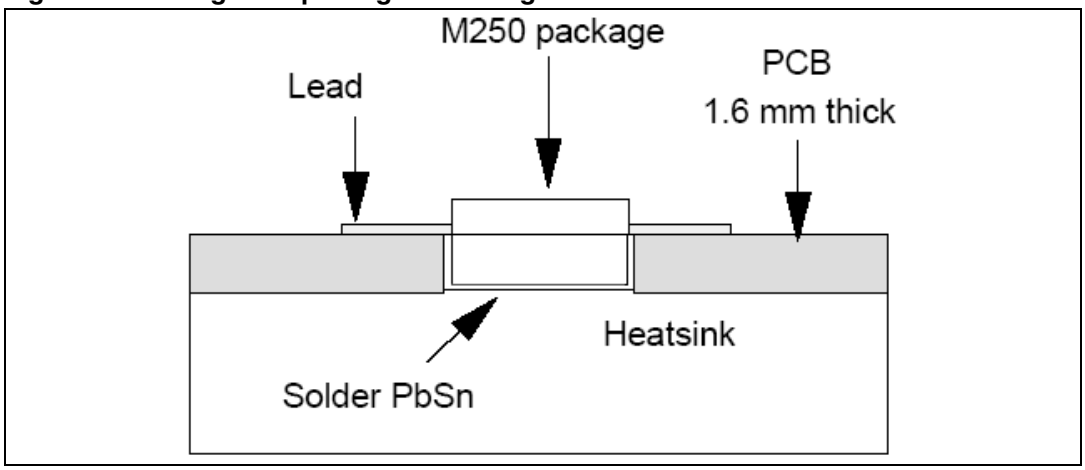


2.1 Flange package (e.g. M243 package)

Heatsink flatness on the mounting area must be better than 0.02 mm. The mounting area roughness must be less than 0.5 µm. Flux solution is not needed. Because the package is non hermetically sealed, damage could occure. The PCB must be thoroughly washed clear of flux solution before mounting the RF transistor. Then a thin layer of thermal paste must be applied to the flange; however, an excessive thickness of thermal paste increases the thermal resistance and caution must be used. Screws with a flat washer must be used in order to apply pressure evenly on the joints. Each screw must be slightly tightened (finger tight: 0.05 Nm) and then the screws must be tightened to the specified torque. A typical torque value for M243 package is 0.65 Nm.

Reflow soldering is the recommended mounting technique even though clamping can also be used. The backside of the package must be directly soldered to the heatsink. (See *Figure 4* for the flangeless package).

Figure 4. Flangeless package mounting



2.2 Flangeless package (e.g. M250 package)

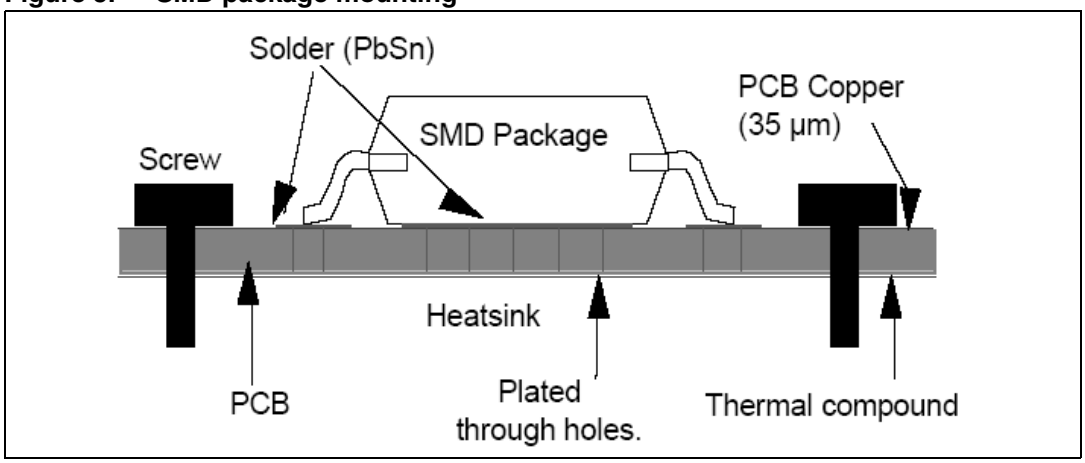
Reflow soldering is the recommended mounting technique even though the clamping method can also be used. The backside of the package must be directly soldered to the heatsink (see *Figure 4*).

2.3 SMD package (e.g. SO-8 ceramic)

Reflow soldering is the recommended mounting technique. Clamping can also be used. Dissipated power (heat) is mainly transferred by conduction from the device to the heatsink through the printed circuit board.

Thermal resistance from the junction to the ambient must be reduced to a minimum value, hence all interfaces between the package and the ambient must be taken carefully into consideration (see *Figure 5*). Metallized ground plate and leads contribute to the heat flow. It is recommended to mount the device on a large grounded metallized area on the printed circuit board. Since the PCB is a poor thermal conductor (FR4, Duroid, etc.), it is also recommended to use thermal vias (plated through holes) to improve heat conduction.

Figure 5. SMD package mounting



3 Lowering the thermal resistance between junction and ambient

In order to decrease the thermal resistance between the junction and the ambient, the following actions may be considered:

1. Increase the number of plated through holes.
2. Increase the holes diameter. However, it must be kept in mind that if the diameter is too large, solder leaks out and forms solder balls beneath the PCB. This increases the thermal resistance between PCB and heatsink (0.5 mm < Hole diameter < 1.0 mm).
3. Decrease spacing between plated through holes.
4. Decrease thickness of the printed circuit board.
5. Use of a thin layer of thermal paste between PCB and heatsink.
6. Screw the PCB to the heatsink as close as possible to the package. The screws also help heat to flow to the heatsink (see *Figure 5*).

4 Revision history

Table 1. Revision history

Date	Revision	Changes
05-Oct-2006	2	Minor text changes
30-Jul-2007	3	The document has been reformatted

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